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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR		ATTORNEY DOCKET NO.
08/808,017	03/03/97	HASHIMOTO	Y	28569.0700

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EXAMINER	
THAI, X	

ART UNIT	PAPER NUMBER
2781	4

DATE MAILED: 09/04/98

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 08/808,017	Applicant(s) Hashimoto et al.
	Examiner Xuan Thai	Group Art Unit 2781

☒ Responsive to communication(s) filed on *Mar 3, 1997*.

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *three* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) *1-10* is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-10* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☒ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐approved ☐disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☒ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☒ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____.

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). *3*

☐ Interview Summary, PTO-413

☒ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

Part III DETAILED ACTION

Specification

1. Claims 1-10 are presented for examination.

2. The Information Disclosure Statement filed 06/04/97 has been received and considered. Please see attached PTO-1449.

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following is suggested: --APPARATUS AND METHOD OF PARTIALLY TRANSFERRING DATA THROUGH BUS AND BUS MASTER CONTROL DEVICE--.

4. The formal drawings submitted on March 03, 1997 have been approved by the Office draftsman. See attached PTO-948.

Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are

such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamasaki et al., hereinafter Yamasaki, (USPN: 5,287,486) in view of Delp et al. (USPN: 5,752,078), hereinafter Delp.

As per claims 1 and 2

Yamasaki teaches the invention as claimed including a method of transferring data through a bus comprising the steps of:

- occupying the bus by a first device serving as a bus master is taught as the DMA controller outputs acknowledge signal DAK to the requesting I/O device 12 which occupying the buses 4-6 for DMA transfer (e.g. see column 1, lines 49-51 and lines 62-68);

- transferring a first determined number of data items of all data items ... while the first device is occupying the bus is taught as the requesting I/O device 12, while occupying the buses 4-6, enters a burst mode for transferring 255 bytes of data directly to RAM 2 (e.g. see column 1, lines 65-68);

- determining if the first device should release the bus based on whether or not there is a request from a second device is taught as when it is determined that there is a refresh request r is inputted during the DMA transfer, the DMA controller 17 stops (e.g. see column 2, lines 1 et seq.);

- releasing the bus by the first device (DMA controller 17) (e.g. see column 2, lines 2-6 and lines 46-50; column 4, lines 43-52);

- occupying the bus by the second device serving as the bus master after the first device releases the bus is taught as after the I/O device (first device) is cut off from the buses, the CPU (second device) is connected to the buses (e.g. see column 2, lines 55-61; column 4, lines 43-46);

- releasing the bus by the second device after the second device completes access to the bus is taught as the buses 4-6 are released (cut-off) from the CPU 1 (second device) after CPU 1 has completed access the buses (e.g. see column 4, lines 17-20;

- occupying the bus again by the first device after the second device releases the bus is taught as the resume procedure in which the I/O device 12 is again connected to the buses 4-6 for transferring the remaining of 255 bytes of data (e.g. see column 20-22);

- transferring a second predetermined of number of data items ... while the first device is occupying the bus again is taught as the remaining of 255 bytes of data is transfer after the resume signal is received (e.g. see column 4, lines 15-24, lines 47-52; and abstract);

Yamasaki, however does not particularly teaches the concept of partial or subset DMA transfer, and determining whether said subset (first predetermined number of data items) have been transferred before releasing the bus to the second device;

It should be noted that partial or subset DMA data transfer is well known and notorious known in the art; for example, Examiner would like to introduce Applicant to the invention of Delp wherein Delp teaches the partial DMA transfer to ensure data transfer integrity. Delp

(figure 5) discloses "block 118, which illustrates making a determination of ***whether the DMA transfer of the packet subset is complete*** (emphasis added). If not, the process returns to block 112. However, if the DMA transfer of the packet subset is complete, the process proceeds from block 118 to block 120, which illustrates making a determination of whether the entire packet has been transferred from adapter memory 44 to user address space. If the DMA transfer of the packet is not complete, the process returns to block 108. However, if the DMA transfer of the packet is complete, the process then proceeds to block 122" (e.g. see figure 5; column 6, line 66 bridging column 7, line 11).

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the current invention was made to utilize the partial or subset DMA transfer and determine whether the transfer have been complete before proceeding to the next task as taught by Delp in the invention of Yamasaki. By doing so, it would first (a) enhancing the data transferring efficiency by always ensuring the number of data items to be successively transferred in a subset, secondly (b) by partially transferring of data during DMA process, it would improve DMA transfer effectiveness, and better correspond to the data processing procedures of the CPU or other I/O devices in Yamasaki's system when interruption routine request occurs during DMA transfer, therefore being advantageous.

As per claim 3

Yamasaki discloses if there is neither DRAM refresh request with high interrupt priority nor external HOLD request (as being equivalent to "the first device should not release the bus"

being claimed), the entire 255 bytes of data are transferred directly to the RAM 2 by the I/O device 12 while it occupies the buses 4-6 (e.g. see column 1, lines 56-68).

As per claim 4

Yamasaki teaches

- determining if all the data items to be transferred have been transferred as ***when the transfer of 255 bytes of data is completed, the transfer counter generates a DMA end signal e*** (emphasis added) (e.g. see column 2, lines 5-7);

- and the further limitation of releasing the bus after it is determined that all the data items to be transferred have been transferred is taught as the I/O 12 is cut off from the buses 4, 5 and 6, which in turn are connected to the CPU 1 after the transfer of 255 bytes of data (e.g. see column 2, lines 12-14);

As per claim 5

Yamasaki teaches the first device is DMA controller 17, and the second device is CPU 1 (e.g. see figure 1);

As per claims 6 and 7

Yamasaki teaches the invention as claimed including a bus master control device for controlling an operation of a bus master for transferring data through a bus, the device comprising:

- bus occupation request means ... is taught as bus request signal generator 10 of DMA controller 17 (e.g. see figure 1, column 1, lines 40-42, lines 52 et seq.);

- data transfer means is taught as the requesting I/O device 12 which enters a burst mode and for transferring 255 bytes of data directly to the RAM 2 (e.g. see column 1, lines 65-68);

- the bus release instruction means is taught as the address output device 3 for releasing the buses 4, 5 and 6 (e.g. see figure 1, column 2, lines 2-3);

- the bus occupation request means (request signal generator 10) outputs again the signal requesting to occupy the bus after the bus release instruction means (address output device 3) outputs the signal instructing to release the bus (e.g. see column 4, lines 15-22);

- the data transfer means transfers a second predetermined number of data items subsequent ... is taught as the I/O device 12 transfers the remaining of the 255 bytes of data to RAM 2 after the data transfer is resumed (e.g. see column 2, lines 17-22);

Yamasaki teaches the invention as claimed except for detailing the concept of partial or subset DMA transfer (transferring a first and second predetermined number of data items);

Again, it should be noted that partial or subset DMA data transfer is well known and notorious known in the art; for example, Examiner would like to introduce Applicant to the invention of Delp wherein Delp teaches the partial DMA transfer to ensure data transfer integrity wherein Delp (figure 5) discloses "block 118, which illustrates making a determination of ***whether the DMA transfer of the packet subset is complete*** (emphasis added). If not, the process returns to block 112. However, if the DMA transfer of the packet subset is complete, the process proceeds from block 118 to block 120, which illustrates making a determination of whether the entire packet has been transferred from adapter memory 44 to user address space. If the DMA

transfer of the packet is not complete, the process returns to block 108. However, if the DMA transfer of the packet is complete, the process then proceeds to block 122" (e.g. see figure 5; column 6, line 66 bridging column 7, line 11).

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the current invention was made to utilize the partial or subset DMA transfer and determine whether the transfer have been complete before proceeding to the next task as taught by Delp in the invention of Yamasaki. By doing so, it would first (a) enhancing the data transferring efficiency by always ensuring the number of data items to be successively transferred in a subset, secondly (b) by partially transferring of data during DMA process, it would improve DMA transfer effectiveness, and better correspond to the data processing procedures of the CPU or other I/O devices in Yamasaki's system when interruption routine request occurs during DMA transfer, therefore being advantageous.

As per claim 8

The further limitation of wherein the bus release instruction means outputs the signal instructing to release the bus after all the data items to be transferred have been transferred is taught by Yamasaki as the address output device 3, when receiving the DMA end signal e for indicating the complete transfer of all 255 bytes of data, the output device 3 releases buses 4, 5 and 6 (e.g. see column 4, lines 17-24 and column 2, lines 2-7);

As per claims 9 and 10

As detailed above with respect to claims 6 and 7, the combination of Yamasaki and Delp disclose the invention as claimed, Yamasaki particularly teaches the transfer counter 9 within the DMA controller 17 for counting a number of data items which have been transferred out of all the data items to be transferred (e.g. see figure 1, and column 1, lines 40 et seq.), and the determination means for determining if all the data items to be transferred have been transferred based on output of the counters is equivalently taught as the DMA end signal e for indicating that 255 bytes of data have been completely transferred (e.g. see column 4, lines 22-24);

The combination of Yamasaki and Delp do not specifically disclose additional counter and determination means for counting a number of data items which have been transferred out of the first predetermination number of data items, and for determining if the first predetermination number of data items have been transferred based on the output of the additional counter;

First, as detailed above with respect to claims 6-7 (as well as claims in 1-2), it would have been obvious to one having ordinary skill in the art at the time the current invention was made to utilize the partial or subset DMA transfer and determine whether the transfer have been completed before proceeding to the next task as taught by Delp in the invention of Yamasaki. Secondly, the counter for counting a number of data items which have been transferred out of the data items to be transferred, and means for indicating whether predetermined number of data have been transferred have been known and disclosed by Yamasaki as detailed above, the additional counter as being claimed is equivalently implemented and performs the same functions as to that of the

disclosed counter of Yamasaki. Accordingly, it would have been obvious to one having ordinary skill in the art at the time the current invention was made to include additional counter for counting a number of data items which have been transferred out of the first predetermination number of data items, and for determining if the first predetermination number of data items have been transferred based on the output of the additional counter, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. *St. Regis Paper Co. vs. Bemis Co.*, 193 USPQ 8.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

8. Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 308-9051 (for formal communications intended for entry)

Or:

(703) 308-6606 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

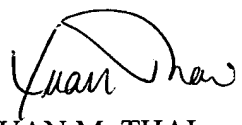
Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Xuan M. Thai whose telephone number is (703) 308-2064.

The examiner can normally be reached on Monday-Thursday from 6:30 AM to 4:00 PM. The examiner can also be reached on alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor Meng-An Ai can be reached on (703) 305-9678.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.



XUAN M. THAI
PATENT EXAMINER
TECHNOLOGY CENTER 2700

XMT
August 31, 1998